REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add two packages, C-5 and C-4. Make changes to table I, and throughout. For case X, the dimensions have been changed and figure 2 has been replaced with the D-10 configuration. Inactivate devices 01XX and 02XX for new design. Add a truth table.	90-01-24	M.A. Frye
B	Add device types 05, 06, 07, and 08. Add vendors CAGES 1ES66, 0H9K9, and 33256. Editorial changes throughout.	93-03-15	M.A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV	B	B	B	B	B														
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS															
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
86-07-10

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, MICROPROCESSOR COMPATIBLE, 12-BIT ANALOG-TO-DIGITAL CONVERTERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-85127**

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-85127	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	574AU	Monolithic, high performance, 12-bit A/D converter with microprocessor interface
02	574AT	Monolithic, medium performance, 12-bit A/D converter with microprocessor interface
03	574AU	Multi-chip, high performance, 12-bit A/D converter with microprocessor interface
04	574AT	Multi-chip, medium performance, 12-bit A/D converter with microprocessor interface
05	574ZA	Monolithic, high performance, low power, 12-bit A/D converter with microprocessor interface
06	574ZB	Monolithic, medium performance, low power, 12-bit A/D converter with microprocessor interface
07	574AU	Monolithic, high performance, low power, 12-bit A/D converter with microprocessor interface
08	574AT	Monolithic, medium performance, low power, 12-bit A/D converter with microprocessor interface

1.2.2 Case outline(s). The case outline(s) shall be as designated MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line
Y	CQCC1-N44	44	square leadless chip carrier
3	CQCC1-N28	28	square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

V_{CC} to digital common	0 to +16.5 V dc
V_{EE} to digital common	0 to -16.5 V dc
V_{LOG} to digital common	0 to +7 V dc
Analog common to digital common:	
device types 01, 02, 03, 04	±1 V dc
device types 05, 06, 07, 08	-0.5 V dc to +1 V dc
Control inputs (CE, CS, A_0, 12/8, R/C) to digital common	-0.5 V dc to V_{LOG} +0.5 V dc
Analog inputs (REF IN, BIP OFF, 10 V_{IN}) to analog common	V_{EE} to V_{CC}
20 V_{IN} analog input voltage to analog common	± 24 V dc
$V_{REF\ OUT}$	Indefinite short to common 10 ms short to V_{CC}
Power dissipation at 75°C:	
Device types 01, 02, 05, 06 , 07, 08	1,000 mW 1/
Device types 03, 04	2,080 mW 1/
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature	-65°C to +150°C

Power dissipation at 75°C:
Device types 01, 02, 05, 06 , 07, 08 - - - - - - - - - - - - 1,000 mW 1/
Device types 03, 04 - 2,080 mW 1/
Lead temperature (soldering, 10 seconds) - - - - - - - - - - +300°C
Storage temperature -65°C to +150°C
Thermal resistance, junction-to-ambient (Θ_{JA}):
Cases X and 3 - 70°C/W
Case Y - 38°C/W
Thermal resistance, junction-to-case (Θ_{JC}) - - - - - - - - - - See MIL-STD-1835
Junction temperature (T_J) - - - - - - - - - - - - - - - - - - +175°C

1.4 Recommended operating conditions.

Power supply
Operating voltage range:
Positive supply (V_{LOG}) - - - - - - - - - - - - - - - - - - +4.5 V dc to +5.5 V dc
Positive supply (V_{CC}) - - - - - - - - - - - - - - - - - - +11.4 V dc to +16.5 V dc
Negative supply (V_{EE}) - - - - - - - - - - - - - - - - - - -11.4 V dc to -16.5 V dc
Ambient operating temperature range (T_A)- - - - - - - - - - - -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

1/ For cases X and 3, derate linearly above T_A = +75°C at 20.8 mW/°C.
For case Y, derate linearly above T_A = +75°C at 22.7 mW/°C.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.2.4 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-1835

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12, for device 01, is used for grading the part selection at 25°C.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Power supply current from V_{LOG}	I_{LOG}		1, 2, 3	01,02, 03,04		40	mA
				05,06, 07,08		1	
Power supply current from V_{CC}	I_{CC}		1, 2, 3	01,02		5	
				03,04		15	
				05,06, 07,08		9	
Power supply current from V_{EE}	I_{EE}		1, 2, 3	01,02, 03,04	-30		
				05,06 07,08	0		
Resolution			1, 2, 3	All	12		Bits
Integral linearity error	ILE		1	All	-0.5	0.5	LSB
			2, 3	All	-1.0	1.0	
Differential linearity error (minimum resolution for which no missing codes guaranteed)	DLE		1	All	12		Bits
			2, 3		12		
Unipolar offset voltage error	V_{IO}	T_A = +25°C	1	All	-2.0	2.0	LSB
			12	01	-1.0	1.0	
Unipolar offset drift	$\frac{\Delta V_{IO}}{\Delta T}$	Using internal reference	2, 3	All	-1.0	1.0	
Bipolar zero offset error	B_Z	T_A = +25°C	1	All	-4.0	4.0	
			12	01	-2.0	2.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Bipolar zero offset drift	$\frac{\Delta B_Z}{\Delta T}$	Using internal reference	2, 3	01,03, 05,07	-1.0	1.0	LSB
				02,04, 06,08	-2.0	2.0	
Gain error	A_E	With 50Ω resistor from REF OUT to REF IN, T_A = +25°C	1	01,02		0.25	% of F.S.
				03,04 05,06 07,08		0.30	
			12	01		0.125	
Gain error drift	$\frac{\Delta A_E}{\Delta T}$	Using internal reference	2, 3	01,03, 05,07	-12.5	12.5	ppm/°C
				02,04, 06,08	-25.0	25.0	
Power supply sensitivity (Maximum change in full scale calibration)	$+P_{SS1}$	+13.5 V $\le V_{CC} \le$ +16.5 V, T_A = +25°C	1	All	-1.0	1.0	LSB
	$+P_{SS2}$	+11.4 V $\le V_{CC} \le$ +12.6 V, T_A = +25°C					
	$+P_{SS3}$	+4.5 V $\le V_{LOG} \le$ +5.5 V, T_A = +25°C	1	All	-0.5	0.5	
	$-P_{SS1}$	-16.5 V $\le V_{EE} \le$ -13.5 V, T_A = +25°C	1	All	-1.0	1.0	
	$-P_{SS2}$	-12.6 V $\le V_{EE} \le$ -11.4 V, T_A = +25°C					
Input impedance	Z_{IN}	10 V span, T_A = +25°C	4	All	3	7	kΩ
		20 V span, T_A = +25°C	4	01,02, 03,04	6	14	
				05,06 07,08	15	25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal reference voltage	V_{REF}	T_A = +25°C 1/	1	01,02	9.98	10.02	V
				03,04 07,08	9.90	10.10	
				05,06	9.97	10.03	
			12	01	9.99	10.01	
Output current 2/	I_O	Available for external loads T_A = +25°C	1	01,02, 03,04		1.5	mA
				05,06 07,08		2.0	
Input voltage (CE, CS, 12/8, R/C, A_0) 3/	V_{IH}	Logic "1" T_A = +25°C	1	01,02, 05,06 07,08	2.0	5.5	V
				03,04	2.4	5.5	
	V_{IL}	Logic "0" T_A = +25°C	1	All	-0.5	0.8	
Input current	I_{IN}	T_A = +25°C	1	01,02 03,04 07,08	-20	+20	µA
				05,06	-1	1	
Output voltage (DB11-DB0, STS)	V_{OL}	Logic "0" T_A = +25°C I_{sink} = +1.6 mA	1	All		0.4	Volts
Output voltage (DB11-DB0)	V_{OH}	Logic "1" T_A = +25°C I_{source} = +500 µA			2.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High impedance state output current	I_Z	High-Z state, T_A = +25°C, DB11 - DB0 only	1	01,02 03,04 07,08	-20	+20	µA
				05,06	-5	+5	
Functional tests		See 4.3.1c, T_A = +25°C	7	All			
Low R/C pulse width 4/	t_{HRL}	See figure 4	9, 10, 11	01,02	250		ns
				03,04	350		
				05,06 07,08	50		
STS delay from R/C 4/	t_{DS}			01,02 03,04		600	
				05,06 07,08		200	
Data valid after R/C low 4/	t_{HDR}			01,02, 05,06 07,08	25		
				03,04	15		
STS delay after valid data 4/	t_{HS}			01,02, 05,06 07,08	300	1000	
				03,04	300	1200	
High R/C pulse width 5/	t_{HRH}			01,02, 03,04	300		
				05,06 07,08	150		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data access time 5/	t_{DDR}	See figure 4	9, 10, 11	01,02, 03,04		250	ns
				05,06 07,08		150	
STS delay from CE 5/	t_{DSC}	See figure 5	9, 10, 11	01,02, 03,04		350	ns
				05,06 07,08		200	
CE pulse width 5/	t_{HEC}			01,02, 03,04	300		
				05,06 07,08	50		
Conversion time 6/	t_C	8-bit cycle		4/ 01,02	10	24	µs
				03,04 05,06 07,08	10	17	
		12-bit cycle		4/ 01,02	15	35	
				03,04 05,06 07,08	15	25	
Access time(from CE)	t_{DD}	See figure 6		01,02		200	ns
4/				03,04		250	
				05,06 07,08		150	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid after CE low 4/	t_{HD}	See figure 6	9, 10, 11	01,02, 05,06 07,08	25		ns
				03,04	15		
Output float delay 4/	t_{HL}	See figure 6	9, 10, 11	01,02		100	
				03,04, 05,06 07,08		150	

1/ The reference voltage external load current shall be a constant dc and shall not exceed 1.5 mA.

2/ Reference should be buffered for operation on ±12 V supplies. External load should not change during conversion.

3/ For devices 01 and 02, $12/\overline{8}$ is not TTL compatible and must be hard wired to V_{LOG} or digital common.

4/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits.

5/ Parameters t_{HRH}, t_{DDR}, t_{DSC}, and t_{HEC}, if not tested, shall be guaranteed to the specified limits.

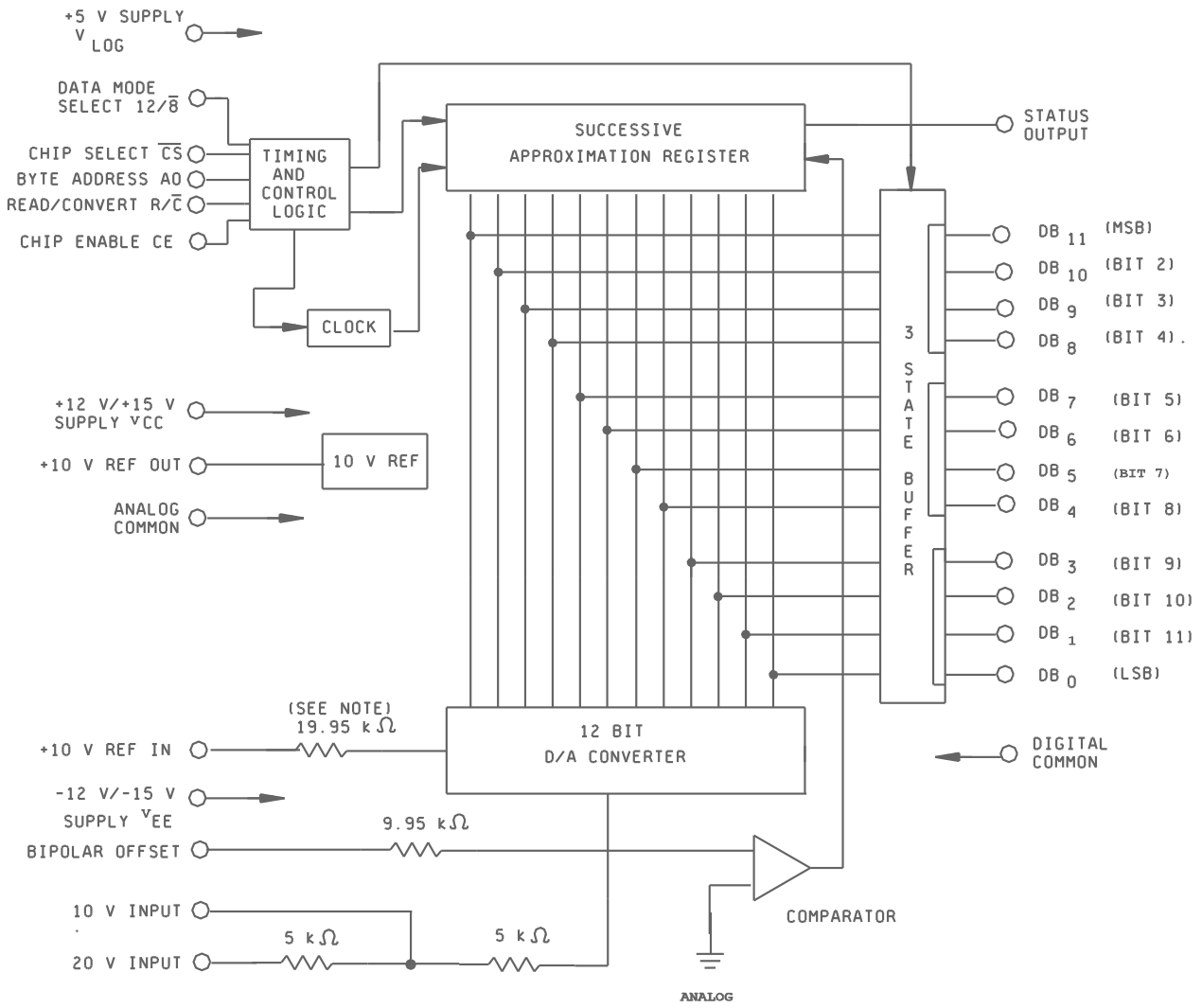
6/ For devices 03 and 04, time is measured from 50 percent level of digital transitions, tested with a 50 pF and 3.0 kΩ load.

Device types	All	01, 02, 05, 06, 07, 08	01, 02, 03, 04
Case outlines	X	3	Y
Terminal number	Terminal symbol	Terminal symbol	Terminal symbol
1	V_{LOG}	V_{LOG}	V_{LOG}
2	12/$\overline{8}$	12/$\overline{8}$	12/$\overline{8}$
3	CS	CS	CS
4	AO_	AO_	AO
5	R/C	R/C	NC
6	CE	CE	NC
7	V_{CC}	V_{CC}	NC
8	REF OUT	REF OUT	NC_
9	AGND	AGND	R/C
10	REF IN	REF IN	CE
11	V_{EE}	V_{EE}	V_{CC}
12	BIP OFF	BIP OFF	REF OUT
13	10 V_{IN}	10 V_{IN}	AGND
14	20 V_{IN}	20 V_{IN}	REF IN
15	DGND	DGND	V_{EE}
16	DB0	DB0	NC
17	DB1	DB1	BIP OFF
18	DB2	DB2	10 V_{IN}
19	DB3	DB3	20 V_{IN}
20	DB4	DB4	NC
21	DB5	DB5	NC
22	DB6	DB6	NC
23	DB7	DB7	NC
24	DB8	DB8	DGND
25	DB9	DB9	NC
26	DB10	DB10	NC
27	DB11 (MSB)	DB11 (MSB)	DB0
28	STS	STS	DB1
29	-	-	DB2
30	-	-	NC
31	-	-	DB3
32	-	-	DB4
33	-	-	DB5
34	-	-	DB6
35	-	-	DB7
36	-	-	DB8
37	-	-	DB9
38	-	-	NC
39	-	-	NC
40	-	-	NC
41	-	-	NC
42	-	-	DB10
43	-	-	DB11 (MSB)
44	-	-	STS

FIGURE 1. Terminal connections.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit parallel output
1	0	1	0	0	Enable 8 most significant bits
1	0	1	0	1	Enable 4 LSBs + 4 trailing zeros

FIGURE 2. Truth table.



NOTE: For device types 03 and 04, the resistor value is 9.95 kΩ.

FIGURE 3. Block diagram.

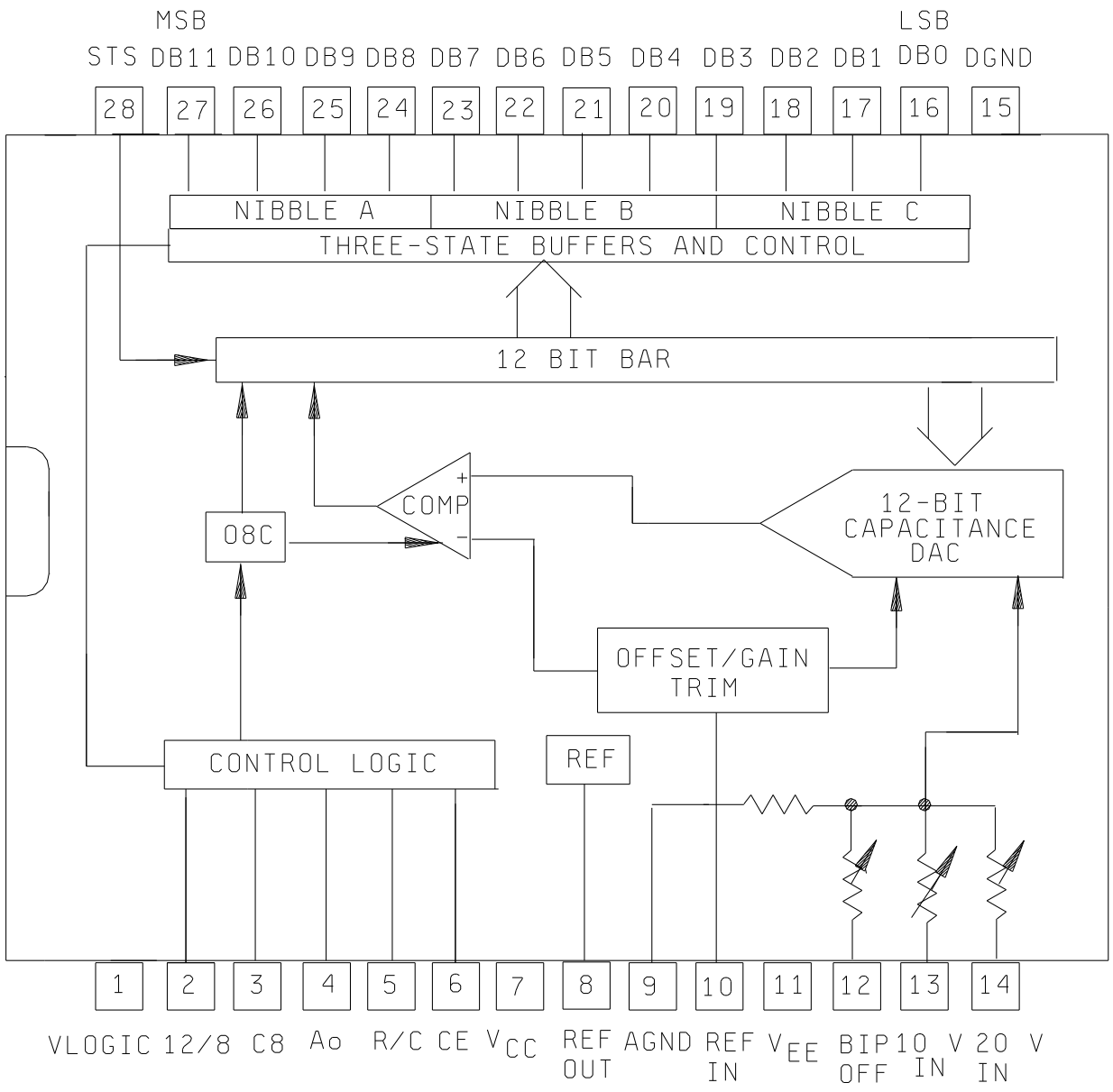
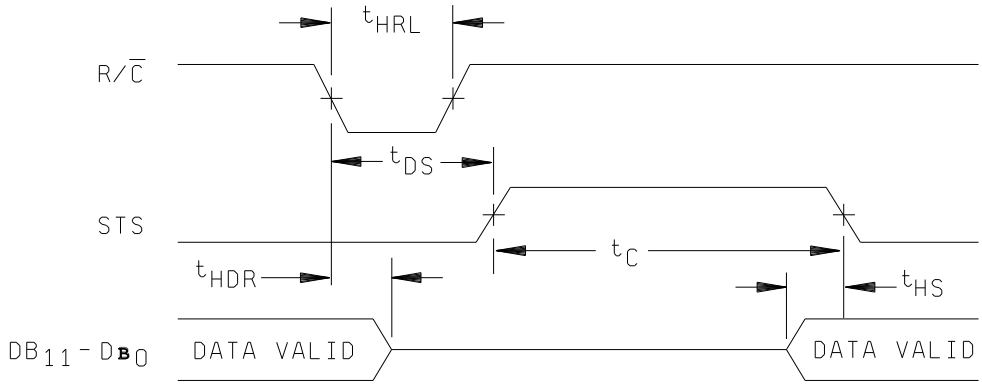
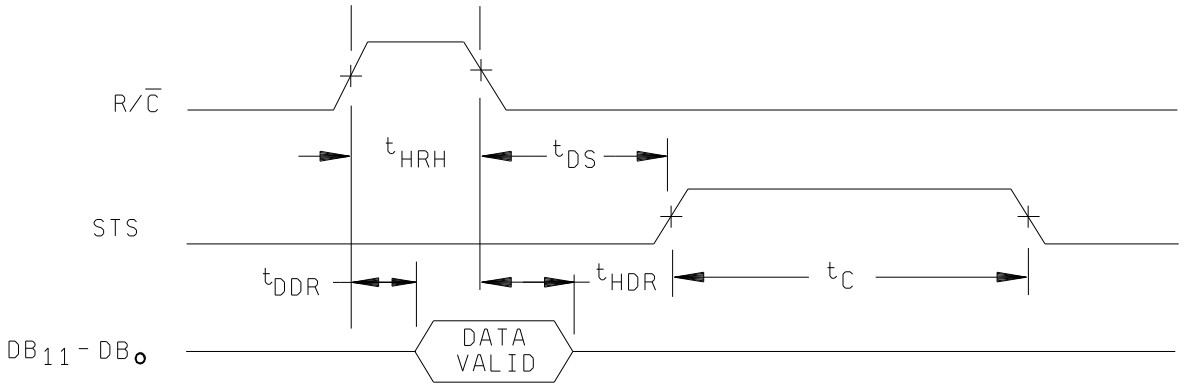


FIGURE 3. Block diagram - Continued.



LOW PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED AFTER CONVERSION



HIGH PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED WHILE R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

FIGURE 4. **High/low pulse for R/$\overline{C}$ outputs**.

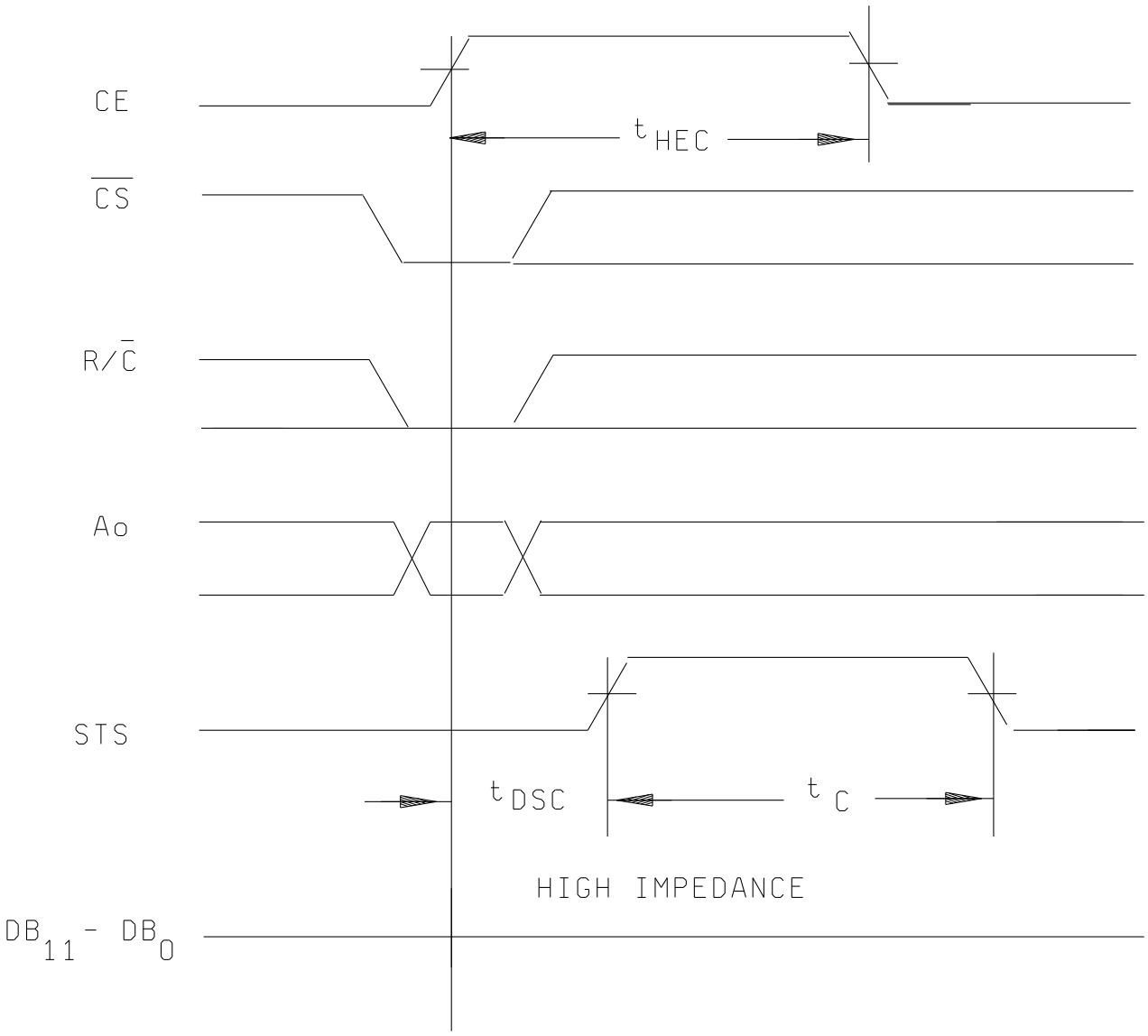


FIGURE 5. Convert start diagram.

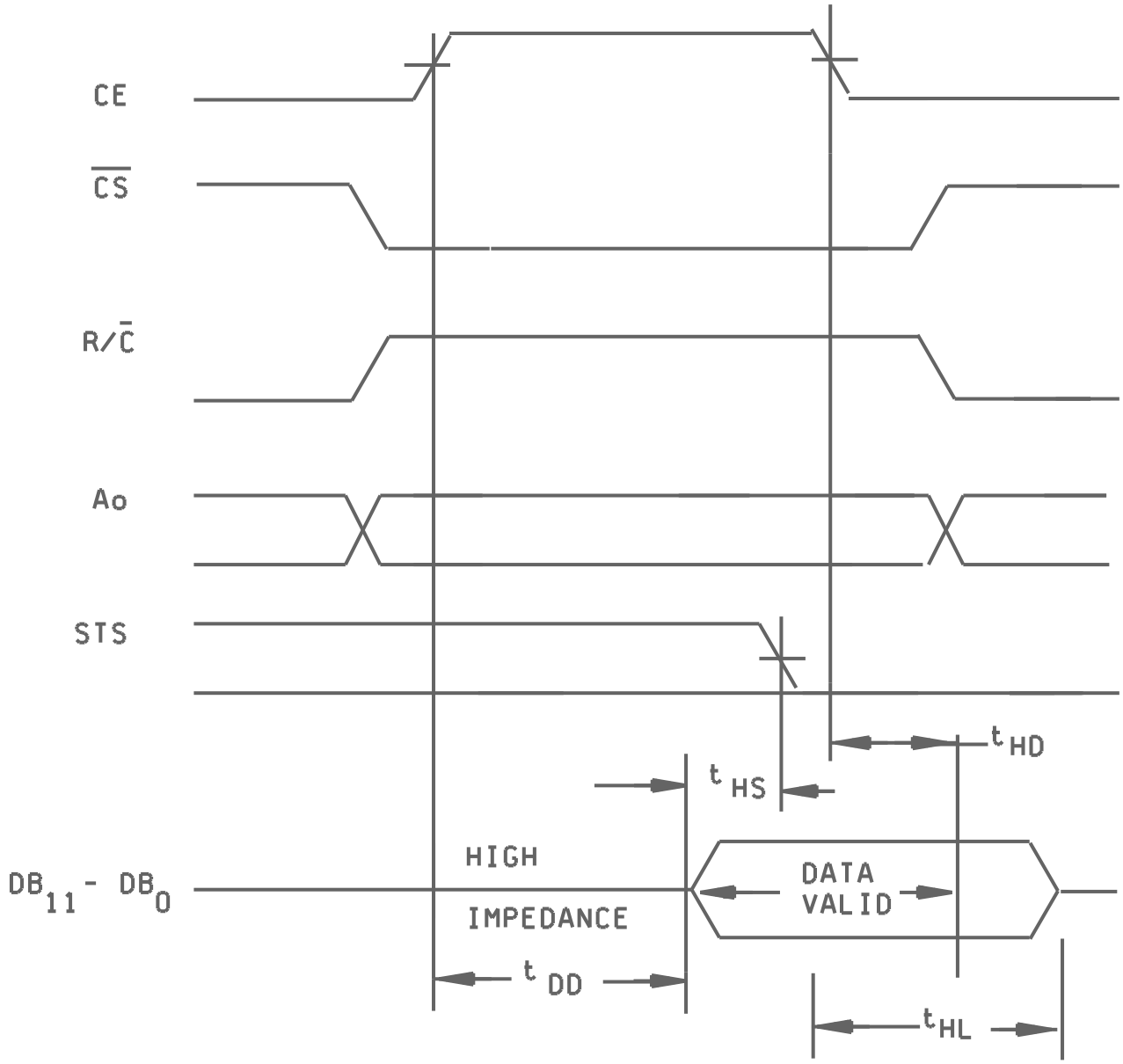


FIGURE 6. **Read cycle timing**.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9 10, 11, 12
Group C and D end-point electrical parameters (method 5005)	1, 4

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

d. Optional subgroup 12, for device 01, is used for grading the part selection at 25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment and manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the devices specified in this drawing will be replaced by the microcircuits identified as PINs M38510/14001 and /14002.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using
DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone
(513) 296-5377.

6.6 Symbols, definitions, and functional descriptions.

V_{LOG}	Logic supply
$\overline{12}/8$	Data mode select input
$\overline{CS}$	Chip select input
$A0$	Byte address/short cycle input
$R/\overline{C}$	Read/convert input
$\overline{CE}$	Chip enable input
V_{CC}	Positive power supply
REF OUT	Reference output
AGND	Analog ground
REF IN	Reference input
V_{EE}	Negative power supply
BIP OFF	Bipolar offset input
V_{IN}	Span input
DGND	Digital ground
D0-D11	Three-state data outputs
STS	Status output
NC	No connection

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in
MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-03-15

Approved sources of supply for SMD 5962-85127 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification PIN
5962-8512701XX 2/	24355 1ES66	AD574AUD/883B MX574AUD/883B OR MX574AUQ/883B	M38510/14001BXX
5962-85127013X	24355	AD574AUE/883B	
5962-8512702XX 2/	24355 1ES66	AD574ATD/883B MX574ATD/883B OR MX574ATQ/883B	M38510/14002BXX
5962-85127023X	24355 1ES66	AD574ATE/883B MX574ATE/883B	
5962-8512703XX	34371	HI1-574AUD/883	M38510/14001BXX 3/
5962-8512703YX	34371	HI4-574AUE/883	
5962-8512704XX	34371	HI1-574ATD/883	M38510/14002BXX 3/
5962-8512704YX	34371	HI4-574ATE/883	
5962-8512705XX	0H9K9	HADC574ZAMJ/883	M38510/14001BXX 3/
5962-85127053X	0H9K9	HADC574ZAMC/883	
5962-8512706XX	0H9K9	HADC574ZBMJ/883	M38510/14002BXX 3/
5962-85127063X	0H9K9	HADC574ZBMC/883	

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification PIN
5962-8512707XX	33256	HS574AU/B	M38510/14001BXX 3/
5962-85127073X	33256	HS574AU/B-LCC	
5962-8512708XX	33256	HS574AT/B	M38510/14002BXX 3/
5962-85127083X	33256	HS574AT/B-LCC	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design. Use QPL M38510 product.

3/ Replacement QPL M38510 device is the recommended substitute for new design.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Incorporated Route 1 Industrial Park PO Box 9106 Norwood, MA 02062-9106 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462
34371	Harris Corporation PO Box 883 Melbourne, FL 32902-0883
1ES66	MAXIM Integrated Products 120 San Gabriel Dr. Sunnyvale, CA 94086-5126
0H9K9	Signal Processing Technologies, Inc 4755 Forge Road Colorado Springs, CO 80907-3519
33256	Sipex Corporation 22 Linnell Circle Billerica, MA 01821-3985